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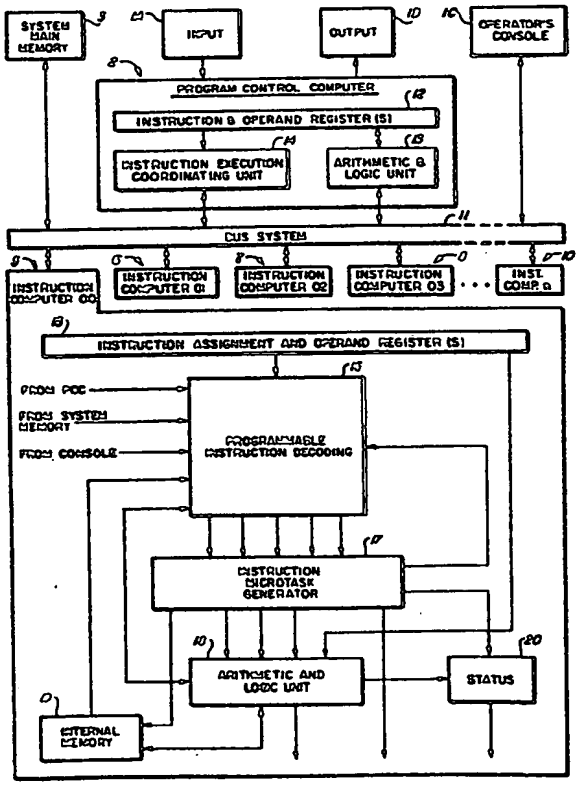
(54) Title: SUPER-COMPUTER SYSTEM ARCHITECTURES

(57) Abstract

A computer system in which instruction sequencing is under the control of a program control computer (2), but each individual instruction is assigned for execution to a individual instruction computer (5-10) in a bank of instruction computers. Each instruction computer includes programmable instruction decoding means (16) by the modification of which the microtasks undertaken to execute an instruction are accordingly modifiable, either between successive execution cycles or during a single execution cycle. Thus, the system has the inherent ability to learn and adapt during the performance of a pr gram. The system may be extended in two-dimensional and three-dimensional arrays to obtain a multiplication of power and to enjoy redundancy advantages.



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SUPER-COMPUTER SYSTEM ARCHITECTURES

Field of the Invention

This invention relates to data processing systems and, more particularly, to computer system architectures which are especially applicable to large scale, powerful systems.

Background of the Invention

Some current and many contemplated applications for large scale, powerful computer systems require tremendous capabilities for computation which continue to push the state of the art in the field for current applications and which far exceed the state of the art for contemplated applications. The performance of computer systems has generally been evolutionary in that the fundamental architecture has remained in a traditional configuration (sometimes called "Von Neumann") involving the sequential execution of instructions which individually are rigidly defined. Even such techniques as parallel processing typically involve arrays of traditionally configured processors functioning under the coordination of a master processor. Virtually all known present and contemplated (insofar as they are disclosed in the literature) system architectures can be analyzed and identified as Von Neumann variations.

One of the present trends for computer system architectures is toward very fast processors having relatively limited command structures. Thus, it is not unlikely that most future computers will be more elementary than those in current use, but will be ultrafast. One significant drawback for this possible evolutionary path is that more and more of the "responsibility" for system performance falls on the softwar , and it is the experienc of the industry that the performanc of many fine computer systems remains software limited. That is, the ultimate p rformance of the systems are limited by inefficiencies which are

simply unavoidable in all but very short programs written in machine language.

Many future applications, such as in artificial intelligence, advanced space technology and the like, impose computational requirements which exceed the ability of traditional Von Neumann systems, no matter how closely the theoretical speed limits are approached, and no matter how configured or arrayed.

Thus, it will be appreciated by those skilled in the art that the fundamental architectural approach for large scale, powerful systems must be rethought if demanding future applications are to be dealt with. It will therefore be commensurately appreciated by those skilled in the art that it would be highly desirable to provide a new architectural structure by the use of which the fundamental and inherent limits of conventional computer systems may be avoided.

Objects of the Invention

It is therefore a broad object of my invention to provide a new computer system architecture.

In another and fundamental aspect, it is an object of my invention to provide a computer system architecture which admits of modification of the computer instruction set.

It is a further object of my invention to provide a computer system architecture in which the computer instruction set can be modified by stored program control.

It is a more specific object of my invention to provide a computer system architecture in which each instruction of the computer instruction set, whose execution is coordinated by a program control computer, is executed by an individual instruction computer.

It is a still further object of my invention to provide means in each instruction computer for modifying the effects of executing a given instruction prior to or during execution.

Summary of the Invention

These and other objects of my invention are achieved by employing a unique computer system architecture in which a program control computer is in communication with a bank of instruction computers. The program control computer includes instruction execution coordinating means which respond to the presence of an instruction in a program sequence by identifying the instruction and selecting an instruction computer to execute the instruction. Each instruction computer includes programmable instruction decoding means which serve to identify the microtasks required for executing a given instruction. The programmable instruction decoding means are further adapted to respond to instruction modification signals applied thereto to change the microtasks identified as necessary for executing the instruction. The programmable instruction decoding means have the ability to dynamically change the precise execution of an instruction, not only between successive execution cycles, but also during a single execution in response to intermediate results. The power of the system may be increased by extending levels in a two-dimensional array and extending the multi-level systems in a three-dimensional array.

Description of the Drawing

The subject matter of the invention is particularly pointed out and distinctly claimed in the concluding portion of the specification. The invention, however, both as to organization and method of operation, may best be understood by reference to the following description taken in conjunction with the subjoined claims and the accompanying drawing of which:

Fig. 1 is a major block diagram of an exemplary computer system employing the present architecture;

Fig. 2 is a more detailed block diagram of the system of Fig. 1; and

Fig. 3 illustrates the extension of the system of Figs. 1 and 2 into multi-level two-dimensional arrays and three-dimensional arrays of multi-level systems.

Detailed Description of the Inventi n

The major block diagram of Fig. 1 illustrates a fundamental aspect of the present invention which sets it apart from prior art data processing system architectures. The system of Fig. 1 includes any suitable aggregation of input/output devices and mediums 1 in communication with a high speed program control computer 2. Also in communication with program control computer 2 is a system main memory 3 which may consist of any assemblage of memory storage means appropriate to a given system application. Both the high speed program control computer 2 and the system main memory 3 are in communication with a bank of instruction computers 4. As few as one instruction computers could comprise the bank 4, but efficient embodiments of the invention preferably include at least as many instruction computers in the bank 4 as there are instructions in the repertoire of the high speed program control computer 2. Thus, the bank of instruction computers 4 illustratively include instruction computer (00) 5, instruction computer (01) 6, instruction computer (02) 7, instruction computer (03) 8, an indeterminate number of instruction computers 9 and instruction computer (n) 10 which represents the final instruction computer in the illustrative bank 4.

It will be understood that the high speed program control computer 2 does not itself execute all the instructions in a program executed by the system, but rather assigns the execution of each instruction in its instruction set to one instruction computer among the bank 4. Merely by way of elementary example, if the instruction "00" in the repertoire of the high speed program control computer 2 is "add one to operand", the program control computer 2 may issue the operand to instruction computer 00 5 along with a signal advising the instruction computer 00 to A) initiate instructi n execution, B) advise the high speed program control computer 2 when execution of the instruction has been

completed (or some meaningful intermediate result has been obtained), and C) return the result to the high speed control computer 2. Other instructions in the repertoire of the high speed program control computer 2 may be executed (serially, in parallel, or both) by the instruction computers comprising the bank 4.

A second fundamental aspect of the architecture of the system comprising the present invention is that, as will be discussed more fully below, means are including in each instruction computer in the bank 4 for altering the meaning and consequent execution of an instruction to be performed (or being performed) by an instruction computer. Thus, returning to the elementary example given above, the instruction "00", which would ordinarily be assigned for execution to instruction computer (00) 5, might have evolved within the instruction computer "00" from an "add one to the operand" to something very much more complex (still by way of example: a macro-instruction such as "find the prime numbers falling between limits a and c") which would better serve performance of the program segment under immediate execution, and the change might be effected within the instruction computer (00) either before or during instruction execution. The source for directing the change in the execution of an instruction may originate from the system program being performed, from human intervention as through an operators' console or from within the assigned instruction computer itself, as through interpretation of intermediate results. Thus, the instruction "00" might be further refined, between executions or during a single execution from intermediate results, to "find the second prime number between the limits b and c, $a < b < c$". Thereafter, when the instruction "00" is sensed during execution of a program by the high speed program control computer 2, that instruction will be so executed until again revised or reinitialized.

Fig. 2 is a more detailed block diagram of the system illustrated in Fig. 1. In Fig. 2, the input/output block has been separated into input 1a, output 1b, and operators' console 1c. The program control computer 2, the system main memory 3 and the illustrated instruction computers 5,6,7,8, and 10 from the bank are all coupled for mutual communication through a comprehensive bus system 11. The operators' console 1c also has access to the bus system 11, and it is contemplated that some embodiments of the invention would be most efficient if the input sub-system 1a and output sub-system 1b had direct access to the bus system 11. The input 1a and the output 1b sub-systems are not of direct import to the fundamental aspects of the present invention and are therefore shown in Fig. 2 as communicating only with the program control computer 2.

High speed program control computer 2 includes instruction and operand register(s) 12 for receiving and temporarily storing instructions and any associated operands from, for example, the system main memory 3. An arithmetic and logic unit 13 in the program control computer 2 communicates with the instruction and operand registers 12, the bus system 11, and an instruction execution coordinating unit 14 which performs supervisory functions pertaining to execution instruction within the system. The instruction execution coordinating unit 14 also accesses the bus system 11 and serves to continually monitor and regulate the relationship between the program control computer 2 and the instruction computers. The instruction execution coordinating unit 14, upon determining the identification of an instruction to be executed in accordance with the currently running program, determines the specific instruction computer to which that instruction is currently assigned for execution, determines the status (i.e., availability or potential availability) of the assigned instruction computer and, when appropriate, causes an indication that the instruction computer is to commence its execution

function operating n such operand information as may be supplied t it via th bus system 11, as may be available from the results of previous execution(s) or both.

The instruction computers comprising the instruction computer bank are, for most contemplated applications, preferably essentially identical to one another; however, this is not a constraint on the inventive system architecture, and it is further contemplated that a hierarchy of instruction computers of differing power may be more appropriate for certain system applications.

Thus, instruction computer (00) 5 includes instruction assignment and operand register(s) 15 for receiving and temporarily storing the information necessary to execute the instruction for which instruction computer (00) 5 is directed and set up to perform. On commencement of execution, a programmable instruction decoding unit 16 is activated and issues signals to instruction microtask generator unit 17. The information contained in the signals applied to the instruction microtask generator unit 17 from the programmable instruction decoding unit 16 depends upon the current decoding configuration of the latter. The instruction microtask generator unit 17 responds to the applied signals by issuing signals representing the microtasks which must be performed in the system to execute the instruction assigned to the instruction computer (00) 5 as currently interpreted by programmable instruction decoding unit 16 in instruction computer (00). These microtask signals are applied, as may be appropriate, to an arithmetic and logic unit 18 in the instruction computer 5, an internal memory 19 in the instruction computer, a status unit 20 in the instruction computer and back to the programmable instruction decoding unit 16 in the instruction computer. Such microtasks, if any, as may be necessary for performance outside the instructi n computer 5 to complet instructi n ex cution are issued to the bus system 11 and communicated to th ir d stination. Preferably, each

instruction computer in the bank is capable of generating a comprehensive set of microtask signals to effect any data manipulation of which the system is capable. Thus, each instruction computer has the inherent ability to perform powerful macro-instructions which may evolve therein.

Arithmetic and logic unit 18, internal memory 19, and programmable instruction decoding unit 16 may all communicate among one another. The arithmetic and logic unit 18 also receives operand information from the instruction assignment and operand register(s) 15, issues signals to the status unit 20 and also is capable of placing information on the bus system 11 for destinations external to the instruction computer 5.

A primary feature of the programmable instruction decoding unit 16 is its programmability. That is, it may be reconfigured to issue a different set of signals to the instruction microtask generator unit 17 whereby a given instruction may be interpreted and executed differently during different instruction cycles. Thus, a programmable instruction decoding unit 16 may be reconfigured under the influence, separately or in conjunction with one another, of external signals from the program control computer, system memory, or from the console under the influence of a programmer. From internal sources, the programmable instruction decoding unit 16 may be reconfigured by signals from the arithmetic and logic unit 18, internal memory 19, and the instruction microtask generator 17.

It will therefore be understood that the actual interpretation and execution of an instruction received by an instruction computer may be varied from execution cycle to execution cycle and, further, that its configuration can be modified during a single execution cycle as a result of the interpretation of intermediate results or for other reasons which render the "adaptation" of the precise execution of the instruction to be desirable.

The significanc of the system architecture presented h rein will now b come more apparent to those skilled in the art. By this system architecture, not only can the system, as a whole, "learn" to execute a program more efficiently, but the instructions themselves can be adapted between successive executions and even during execution. Because of this ability to learn and adapt, the spread of system responsibility between software and hardware can be optimized; i.e., the system becomes less software-bound since the software need not be as complex and detailed as with traditional high speed computer systems in which the "definition" of individual instructions remains fixed or only slightly modifiable within strict and predetermined limits.

The actual logical design of several constituents of the system illustrated in Fig. 1 and 2, particularly those of the program control computer 2 and the instruction computers in the bank 4 as exemplified by the instruction computer 5, straightforwardly follow their function and can be carried out according to conventional techniques. It may be noted that the operating systems employed, respectively, in the program control computer 2 and in the instruction computers need not necessarily be the same. An instruction computer need only be furnished with operand-like information if necessary, instruction modification information if applicable, and an indication that it is to commence undertaking its internally defined and adaptable instruction sequence and have the results available when completed (or at an intermediate point) as indicated by the status unit 20. Therefore, the instruction computers, operating at a different level from the program control computer, are somewhat independent and can use an operating system optimum for their structure as chosen by the logic and circuit designers.

Communication (over the bus system 11 and otherwise such as in dedicated channels) between the various system constituents may b perf rmed in parallel, in seri s or

in a combination series/parallel manner as, again, the detailed design of an individual system may prescribe.

The system shown in Fig. 2 is essentially uni-dimensional in that there is shown only a single program control computer, a single bank of instruction computers, and a single level of main memory and input/output. However, the system architecture is especially well adapted for integration into very large scale two-dimensional and three-dimensional supersystems particularly including those subject to reconfiguration under program control. Referring now to Fig. 3, representations of such supersystems employing extensions of the architecture of the present invention are presented. It will be seen in Fig. 3 that multi-level system (0) 25 comprises a series of program control computers 26 disposed in levels 0-p. Similarly, a series of instruction computer banks 27 are disposed at levels 0-m and a series of system memories 28 are disposed at levels 0-1. (Thus, each level of the multi-level system 25 comprises much of the structure illustrated in Fig. 2.) Communication both within a level and among different system levels may be carried out across a three-dimensional multi-bus system 29. Input/output 30 may be coupled into the system at one or more levels, typically interfacing either with the multi-bus system 29 or one or more program control computers.

The two-dimensional supersystem comprising multi-level system 0 may be further extended by interfacing the multi-bus system 29 with additional multi-level systems 1-q 31. It will be apparent that, under program control, the instruction computers at different levels in multi-level system (0) 25 can be accessed by the program control computers 26 and memories 28 at diverse levels in order to achieve not only redundancy, but the ability to adapt to a complex problem virtually to the extent of realizing the equivalent of a hard-wired, completely special purpose system. The provision of additional

multi-level syst ms 31, within practical limits, further extends the system power to adapt.

In a multi-level system, one program control computer must generally be dominant in order to direct system reconfiguration as may be useful and to resolve conflicts which may arise from, for example, attempts by multiple program control computers to access a given instruction computer. Similarly, in a three-dimensional system including a plurality of multi-level systems, a hierarchy must be established, and a single program control computer will be the ultimate arbiter.

Referring again to Fig. 2, it will be noted that system initialization is a substantial event because each of the instruction computers must be made aware of its initial instruction decoding configuration. Initialization may be performed by running, in the program control computer 2, an initialization program which assigns to each instruction computer in the instruction computer bank its beginning instruction sequence. Alternatively, an initialization signal may be applied to each instruction computer which has permanently stored therein (as in internal memory 19) the key to its initial instruction decoding. For achieving the most flexibility and for providing redundant capability against the failure of one or more instruction computers, the former procedure is preferred.

As previously noted, the logical design of individual computer systems employing the novel architecture set forth herein is susceptible to performance using standard techniques and will vary according to the system size, intended application, logic family chosen, etc.

Therefore, while the principles of the invention have now been made clear in an illustrative embodiment, th re will be obvious, to those skilled in the art, many modifications of structure, arrangements, proportions, and the elements us d in the practice of th invention which are particularly adapted for specific environments

and op rating requirements without departing from those principles.

I CLAIM:

1. A data processing system including:

A. a program control computer;

B. a bank of instruction computers;

C. means coupling said program control computer and each instruction computer in said bank for communication therebetween;

D. instruction execution coordinating means included in said program control computer and adapted to transfer a signal representing an identified instruction to one of said instruction computers; and

E. programmable instruction decoding means included in at least one of said instruction computers for receiving a signal representing an instruction and for responding thereto by generating microtask signals representative of the tasks required for executing the instruction, said programmable instruction decoding means being further adapted to respond to instruction modification signals applied thereto by changing the microtask signals generated thereby.

2. The data processing system of Claim 1 in which each instruction in an instruction set of said program control computer is assigned to an instruction computer in said bank and in which each said instruction computer in said bank includes programmable instruction decoding means for receiving a signal representing said assigned unique instruction and for responding thereto by generating microtask signals representing the tasks required for executing said assigned unique instruction, each said programmable instruction decoding means being further adapted to respond to instruction modification signals applied thereto by changing the microtask signals gen rated thereby.

3. The data processing system of Claim 2 in which said program control computer includes means responsive to system initialization for generating a group of predetermined instruction modification signal sets and for transferring a predetermined one of said instruction modification signal sets to said programmable instruction decoding means in each said instruction computer in said bank to establish initial microtask signals generated thereby in response to a signal representing said unique instruction assigned to each said instruction computer.

4. The data processing system of Claim 2 in which each said instruction computer includes feedback means for selectively responding to intermediate results obtained during the execution of an instruction for issuing instruction modification signals to said programmable instruction decoding means included therein whereby microtask signals generated by said programmable instruction decoding means are changed during instruction execution.

5. The data processing system of Claim 1 which further includes a main system memory, in which said coupling means comprises a bus system and in which said program control computer, said main system memory, and each of said instruction computers have access to said bus system for communication thereamong.

6. The data processing system of Claim 2 which further includes a main system memory, in which said coupling means comprises a bus system and in which said program control computer, said main system memory, and each of said instruction computers have access to said bus system for communication thereamong.

7. Th data processing system of Claim 3 which further includes a main system memory, in which said coupling means comprises a bus system and in which said program

control computer, said main system memory, and each of said instruction computers have access to said bus system for communication thereamong.

8. The data processing system of Claim 4 which further includes a main system memory, in which said coupling means comprises a bus system and in which said program control computer, said main system memory, and each of said instruction computers have access to said bus system for communication thereamong.

9. A data processing system including:

A. a plurality of program control computers;

B. a supervisory computer;

C. a plurality of instruction computer banks, each of said instruction computer banks comprising a plurality of instruction computers;

D. a plurality of system memories;

E. a bus system coupling said program control computers, said supervisory computer, said system memories and said instruction computers for communication thereamong;

F. instruction execution coordinating means included in each of said program control computers and adapted to transfer a signal representing an identified instruction to one of said instruction computers; and

G. programmable instruction decoding means included in each of said instruction computers for receiving a signal representing an instruction to be executed and for responding thereto by generating microtask signals representative of the tasks required for executing the instruction, said programmable instruction decoding means being further adapted to respond to instruction modification signals applied thereto by changing the microtask signals generated thereby.

10. The data processing system of Claim 9 in which said supervisory computer is a selected one of said program control computers.

11. The data processing system of Claim 9 in which each said instruction computer includes feedback means for selectively responding to intermediate results obtained during the execution of an instruction for issuing instruction modification signals to said programmable instruction decoding means included therein whereby microtask signals generated by said programmable instruction decoding means are changed during instruction execution.

12. The data processing system of Claim 10 in which each said instruction computer includes feedback means for selectively responding to intermediate results obtained during the execution of an instruction for issuing instruction modification signals to said programmable instruction decoding means included therein whereby microtask signals generated by said programmable instruction decoding means are changed during instruction execution.

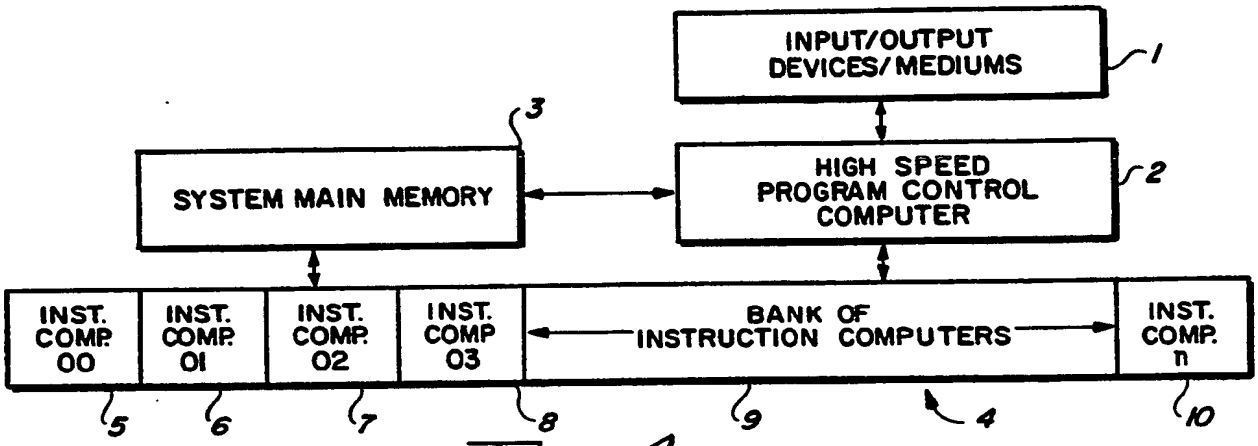

Fig. 1

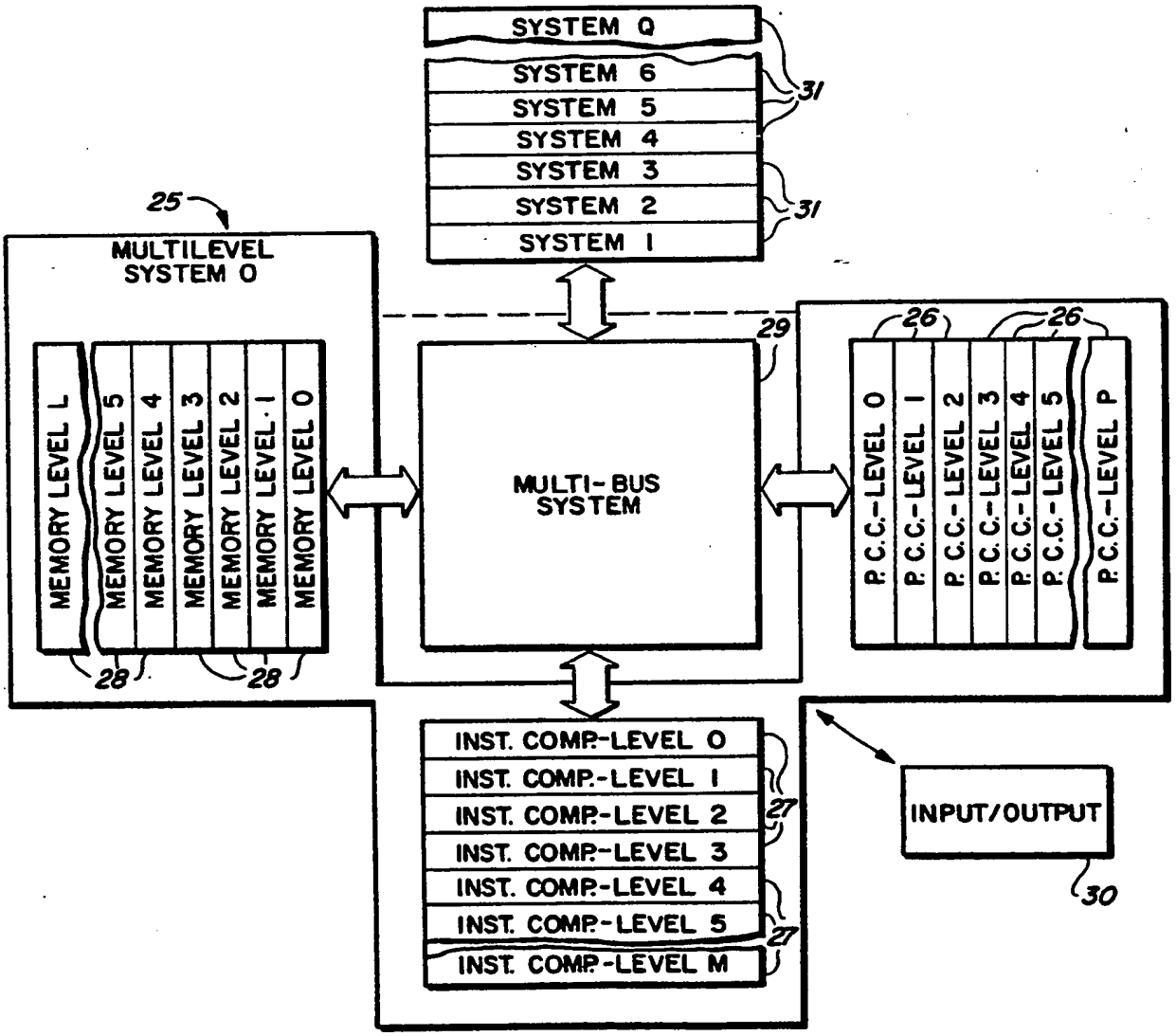

Fig. 3

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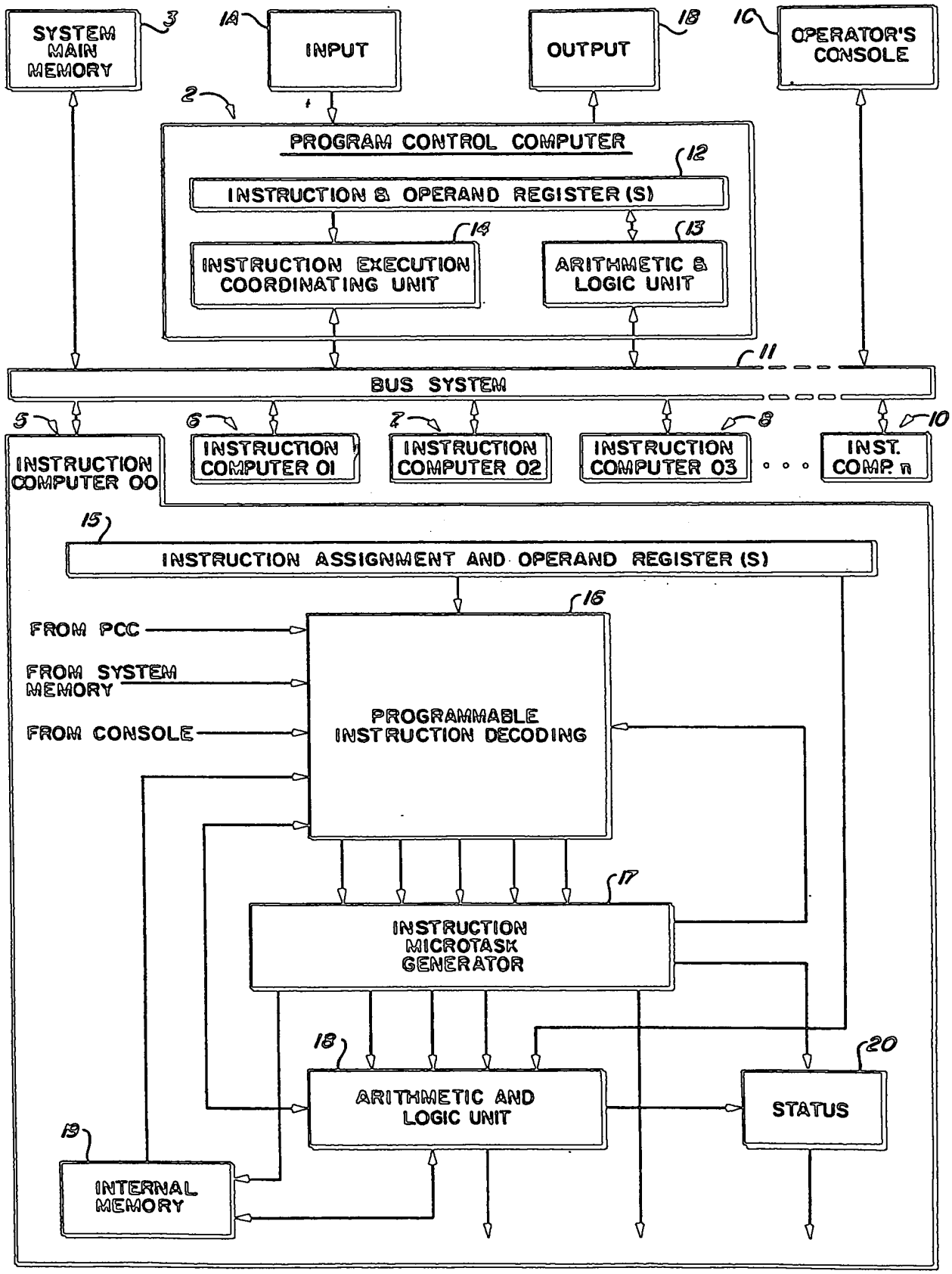

FIG-2

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INTERNATIONAL SEARCH REPORT

International Application No PCT/US 85/01435

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: G 06 F 9/38; G 06 F 15/06

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	G 06 F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	EP, A, 0121763 (M.S. GREGORY et al.) 17 October 1984 see page 8, line 22 - page 12, line 14 and page 22, lines 13-34 --	1,2,4-6,8
Y	US, A, 3308436 (W.C. BORCK et al.) 7 March 1967 see column 3, line 3 - column 5, line 54 --	1,2,4-6,8
A	DE, A, 2425380 (G. URSCHLER) 27 February 1975 see page 5, last paragraph; page 6; page 12, paragraph 2 - page 20, paragraph 1 --	1,5
A	EP, A1, 0077404 (M. KURAKAKE) 27 April 1983 see page 5, line 13 - page 6, line 11 --	1-3
A	Proceedings of the 1983 International	./.

* Special categories of cited documents: [10]

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
9th October 1986	21 NOV 1986
International Searching Authority	**Signature of Authorized Officer**
EUROPEAN PATENT OFFICE	M. VAN MOL

Form PCT/ISA/210 (second sheet) (January 1985)

III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET)

Category °	Citation of Document, with indication, where appropriate, of the relevant passages	Relevant to Claim No
	Conference on Parallel Processing 23-26 August 1983, IEEE (New York, US) G. Fritsch et al.: "EMSY 85 The erlangen multiprocessor system for a broad spectrum of applications", pages 325-330, see page 326, left-hand column	9-12

Form PCT ISA/210 (extra sheet) (January 1985)

ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 85/01435 (SA 13698)

This Annex lists the patent family members relating to the patent documents cited in the above-mentioned international search report. The members are as contained in the European Patent Office EDP file on 22/10/86

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Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A- 0121763	17/10/84	AU-A-	2527584	13/09/84
		JP-A-	59223874	15/12/84
		US-A-	4580215	01/04/86
		CA-A-	1209711	12/08/86
		US-A-	4546428	08/10/85
US-A- 3308436		GB-A-	1026890	
		DE-A-	1238695	
		FR-A-	1420405	
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		AT-A,B	335202	25/02/77
		JP-A-	50040243	12/04/75
EP-A- 0077404	27/04/83	WO-A-	8203708	28/10/82
		JP-A-	57176456	29/10/82

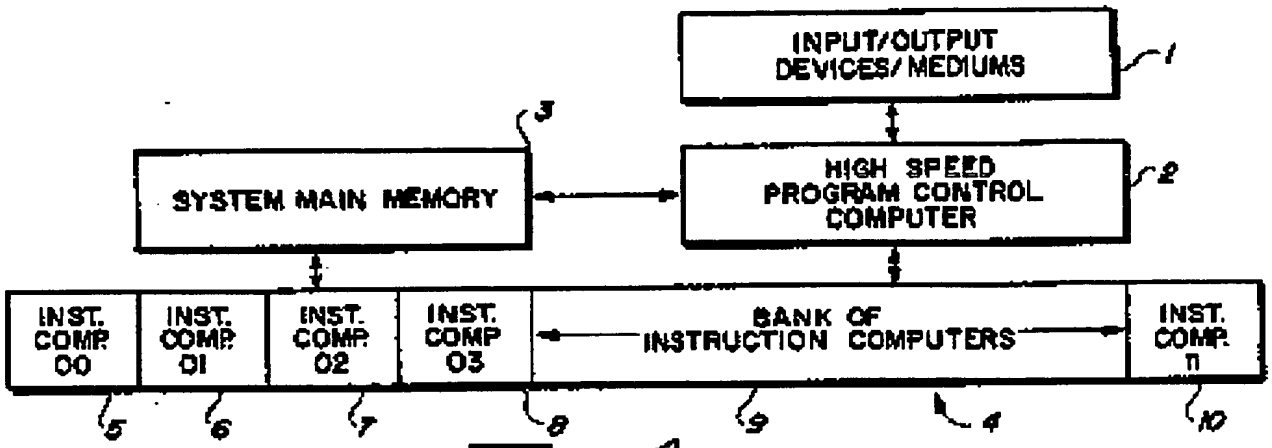

Fig-1

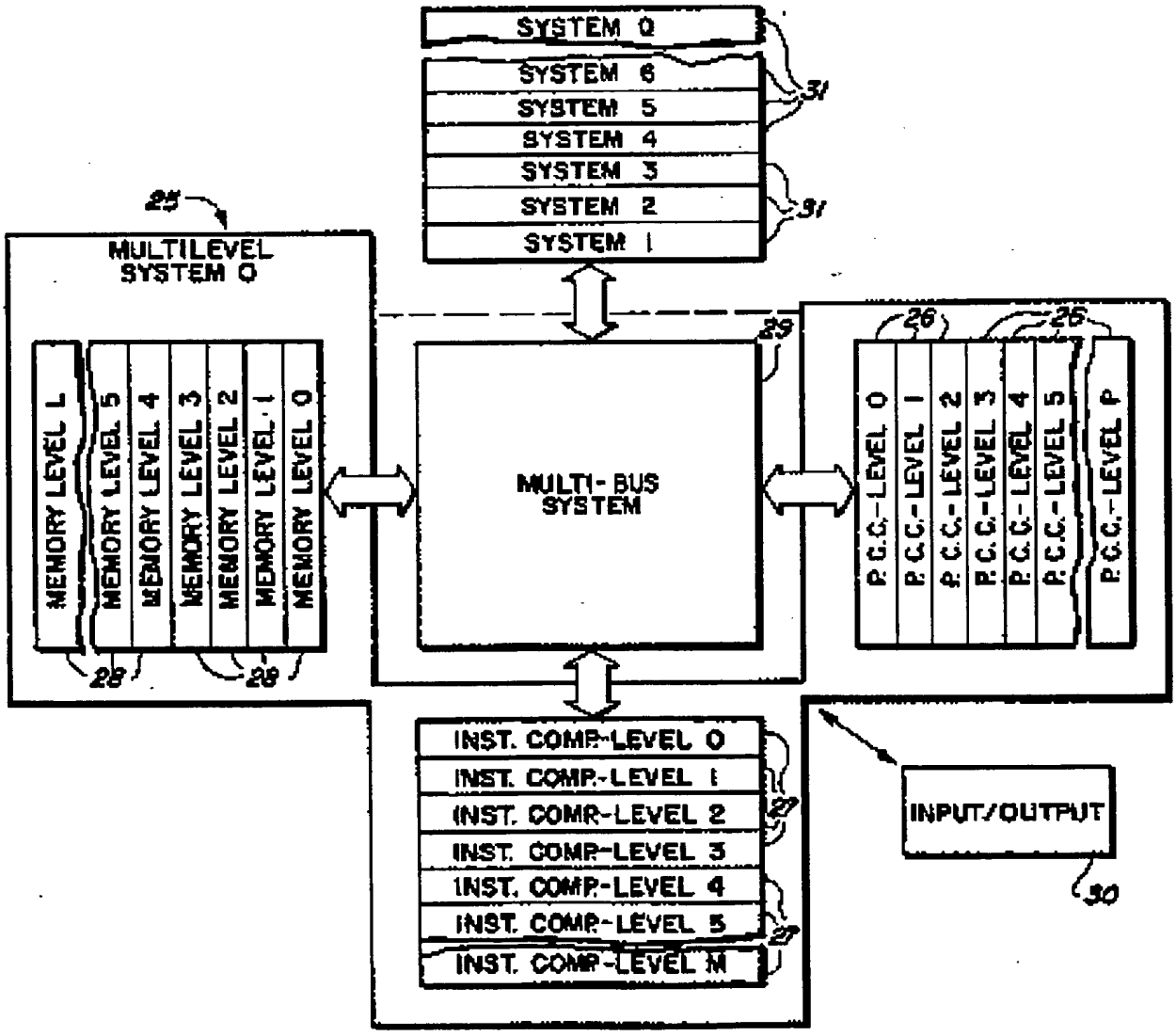

Fig-3

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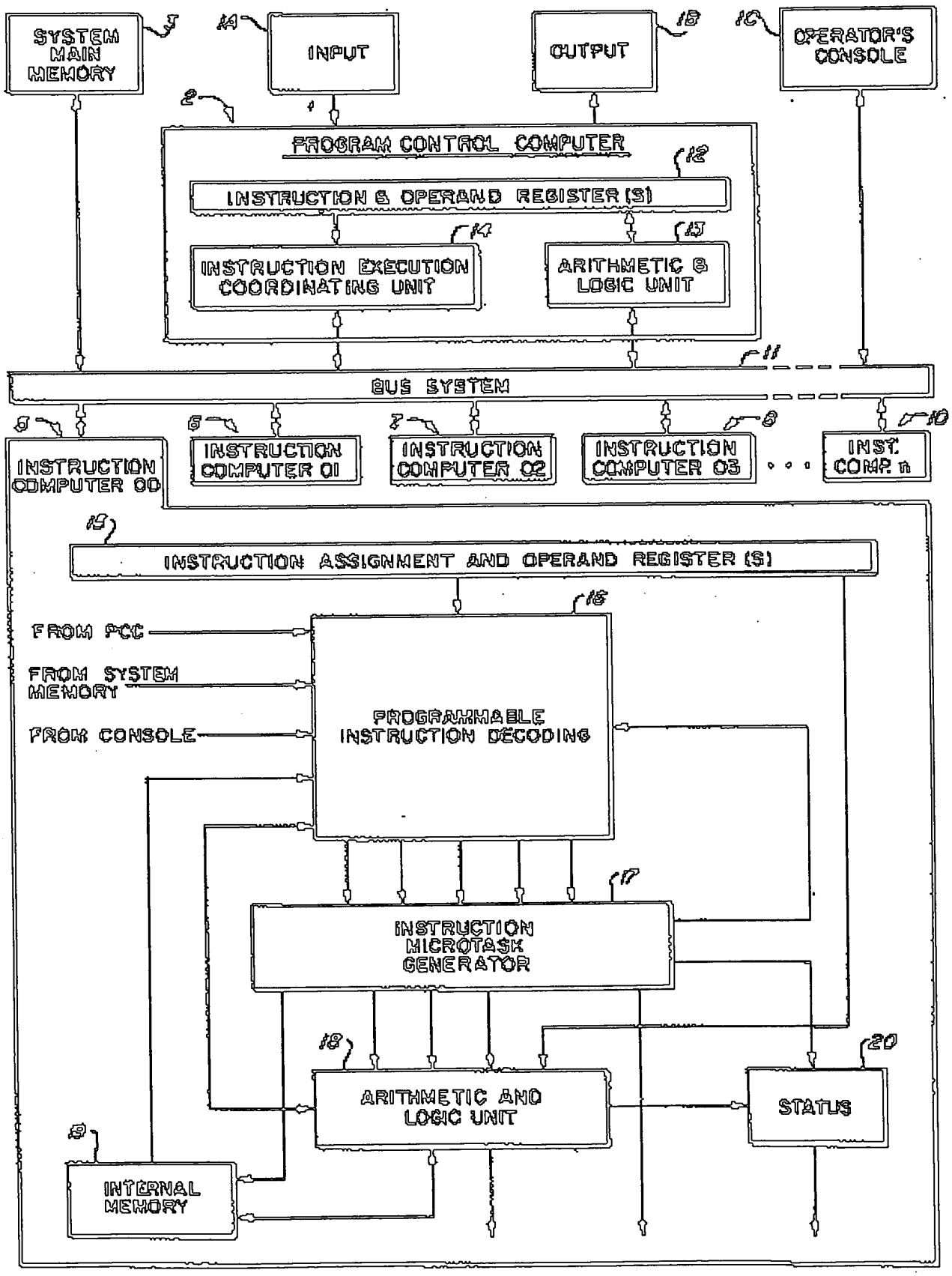

Fig. 2

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